1. Understand:

* Operating System
* Compilers
* Embedded systems development
* Make decisions about computer purchase

1. Controls CPU; Sequences execution of instructions; Causes transfers of register data; Control unit implemented using a program rather than by sequential logic or using microinstructions
2. Does not need to charge capacitors to drive signals outside chip; length of signal path
3. Software on older processors works on newer generations
4. Speed limited by the amount of sequential code; Speedup of N processors = 1/((1-f)+f/N) where f is the parallelizable fraction
5. CPI = 1\*0.45 + 2\*0.34 + 3\*0.15 + 2\*0.07 = 1.72; MIPS = 1470
6. More aggregate throughput; match devices to speed of bus; No contention; No propagation delays
7. (a) Higher priority interrupt; Nested (b) can preempt lower priority; sequential handling; pending upon flag
8. (a)Spatial tendency of a program to access sequential contiguous locations (b) Temporal tendency of a program to access most recent locations (c) for (i=0;i<10;i++) for(j=0; j<10; j++) a[i] = a[i]\*j; Outer loop – Spatial, Inner loop – Temporal; Implications - caching
9. Addresses map to a unique line; only one line to evict
10. Unified – Bigger cache for either code and data, so if size of code is not equal to size of data, can accommodate better and eliminate contention between instructions and data; Split cache – Separate locality for code and data
11. Write though:(-)Bus bottleneck (congestion) (-)Slower, since need to updated both (+)coherence ; Write back: (-) Coherence must be handled (+) Merging writes minimizes slower memory writes
12. Tag field is 12 bits
13. Set field is 10 bits
14. Word field is 2 bits
15. No. Because the circuitry supports self-charging a single 6T cell.
16. Single bit errors detected using parity; Single bit errors located and corrected using hamming code; No.